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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,691	07/27/2006	Hannes P. Hofmann	EFFEP0101US	7045

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EXAMINER	
NGUYEN, HUNG D	
ART UNIT	PAPER NUMBER
3742	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/587,691	HOFMANN, HANNES P.	
	Examiner	Art Unit	
	HUNG NGUYEN	3742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/5/2010, 4/8/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. In claim 1, there is insufficient antecedent basis for "the circuit board" recited in line 5 in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 10, 12-14, 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clothier et al. (US Pub. 2002/0177006) in view of Asai et al. (US Pat. 6,240,636) (both newly cited).

6. Regarding claim 1, Clothier et al. discloses a structure having flush circuitry features and method of making comprising: providing a carrier foil (1, Fig. 2a) ; coating the carrier foil (1, Fig. 2A) on at least one side thereof with a dielectric (3, Fig. 2C) to form a dielectric layer; structuring the dielectric layer for producing trenches 4 (Fig. 2C) therein using laser ablation (Par. 42), the trenches not extending completely through the

dielectric layer to the circuit traces and the vias extending through the dielectric layer to the circuit traces (Fig. 2C shown the trenches not extending completely through the dielectric layer 3); depositing a primer onto the entire surface of the dielectric layer or depositing the primer layer into the produced trenches (Par. 45); depositing a metal layer (5, Fig. 2D) onto the primer layer, with the trenches being completely filled with metal for forming conductor structures therein; removing the metal layer (Fig. 2E) and the primer layer, except for in the trenches and vias, to expose the dielectric layer if the primer layer has been deposited onto the entire surface in method step.

Clothier does not disclose providing a printed circuit board having a circuit traces on at least one side thereof; structuring the dielectric layer for producing vias; and the vias extending through the dielectric layer to the circuit traces. Asai et al. discloses providing a printed circuit board (Fig. 1) having a circuit traces (3, Fig. 1) on at least one side thereof and structuring the dielectric layer for producing vias (5, Fig.1) using laser ablation; and the vias (5, Fig. 1) extending through the dielectric layer to the circuit traces. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in Clothier et al., providing a printed circuit board having a circuit traces on at least one side thereof; structuring the dielectric layer for producing vias; and the vias extending through the dielectric layer to the circuit traces, as taught by Asai et al., in order to fabricate multilayer interconnect printed circuit board.

7. Regarding claim 10, Clothier further discloses further method steps are performed one or several times after method step (f); depositing another dielectric layer

onto the dielectric layer being provided with trenched and vias; and repeating the step © through (f) (Par. 51)

8. Regarding claim 12, Clothier et al. further discloses the primer layer is deposited by sputtering or by a direct deposition method (Par. 45-46).

9. Regarding claim 13, Clothier et al. further discloses a method of manufacturing printed circuit board wherein the metal layer is formed by electroless plating (Par. 45-46).

10. Regarding claim 14, Clothier et al. further discloses a method of manufacturing printed circuit board wherein the metal layer and the primer layer are removed by polishing (Par. 47).

11. Regarding claim 21, Clothier et al. further discloses a method of manufacturing printed circuit board wherein a method of manufacturing printed circuit board where the printed circuit board is a multilayer circuit board comprising two sides and a conductor pattern on each side (Fig. 2).

12. Regarding claim 24, Asai et al. further discloses the laser ablation comprises contacting the dielectric layer with reactive gas during the laser ablation (Fig. 1).

13. Claims 2-11, 15 and 18-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Clothier et al. (US Pub. 2002/0177006) in view of Asai et al. (US Pat. 6,240,636) and further view Tamm et al. (US Pat. 5,666,722) (Previously cited).

14. Regarding claim 2, Clothier/Asai disclose substantially all features of the claimed invention as set forth above **except** the trenches and vias are produced in one single process operation in method step. Tamm discloses trenches (24, 25 and 26 Fig. 2b)

and vias (23a, Fig. 2c) are produced in one single process operation in method step (Col. 4, Lines 50-54; Col. 4, Line 66 to Col. 5, Line 2). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in Clothier/Asai, the trenches and vias are produced in one single process operation in method step, as taught by Tamm et al., in order to simplify the process of manufacturing the printed circuit board.

15. Regarding claim 3 and 20, Tamm further discloses a method of manufacturing printed circuit board where the trenches and vias are performed by a laser ablation with direct-writing technique (Col. 6, Lines 17-24).

16. Regarding claim 4, Tamm further discloses a method of manufacturing printed circuit board where the direct-write technique comprises scanning a laser beam across the dielectric layer at those surface regions of the dielectric in which the trenches and vias are to be produced (Col. 6, Lines 17-45).

17. Regarding claims 5 and 18, Tamm further discloses a method of manufacturing printed circuit board which adjusting the power of the laser beam to depend on the depth of the trenches and vias to be produced (Col. 3, Lines 38-40; Col. 6, Lines 45-47).

18. Regarding claim 6, Tamm further discloses a method of manufacturing printed circuit board where the direct-write technique further comprises pulsing the laser beam (Col. 3, Lines 29-33).

19. Regarding claim 7, Tamm further discloses a method of manufacturing printed circuit board where adjusting the energy amount of the laser beam irradiated to a surface area of the dielectric layer to depend on the depth of the trenches and vias to be

produced by setting the number of laser pulses being irradiated to said surface area (Col. 3, Line 38-43).

20. Regarding claims 8 and 22, Tamm further discloses a method of manufacturing printed circuit board where the direct-write technique further comprises decreasing the energy amount of successive energy pulses being irradiated to a surface area of the dielectric layer (Col. 3, Line 38-43).

21. Regarding claim 9, Tamm further discloses a method of manufacturing printed circuit board where the trenches are connected to another trenches in different layers for multilayer board (Fig. 2f).

22. Regarding claim 10, Tamm further discloses a method wherein further method steps are performed once or several times after method step f): g) Depositing another dielectric layer onto the dielectric layer being provided with trenches and vias; and h) Repeating the steps c through f (Fig. 1g; Col. 4, Lines 42-49).

23. Regarding claims 11 and 19, Tamm further discloses a method of manufacturing printed circuit board wherein a terminating layer 12 and 13 (Fig. 1g) is deposited after any one of method steps f or h (Col. 4, Lines 42-49).

24. Regarding claim 15, Tamm further discloses a method of manufacturing printed circuit board wherein producing trenches and vias in the dielectric in method step c comprises producing trenches, said trenches also comprising vias (Fig. 2b-2c).

25. Regarding claim 21, Tamm further discloses a method of manufacturing printed circuit board wherein a method of manufacturing printed circuit board where the printed

circuit board is a multilayer circuit board comprising two sides and a conductor pattern on each side (Fig. 2f) (Col. 4, Lines 32-35).

26. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clothier et al. (US Pub. 2002/0177006) in view of Asai et al. (US Pat. 6,240,636) and further view of Konrad et al. (US Pub. 2002/0129972) (Previously cited).

27. Regarding claim 16, Clothier/Asai disclose substantially all features of the claimed invention as set forth above **except** the functional layers are deposited onto the metal layer for electrically contacting electric components. Konrad et al. discloses the functional layers are deposited onto the metal layer for electrically contacting electric components (Par. 49). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in Clothier/Asai, the functional layers are deposited onto the metal layer for electrically contacting electric components, as taught by Konrad et al., in order to have a excellent conductive layer that makes contact with semiconductor chip.

28. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clothier et al. (US Pub. 2002/0177006) in view of Asai et al. (US Pat. 6,240,636) and further view of Yokogawa et al. (US Pat. 6,740,416) (Previously cited).

29. Regarding claim 17, Clothier/Asai disclose all the claimed features as set forth above **except** the circuit carrier is manufactured in a horizontal line. Yokogawa et al. discloses the circuit carrier is manufactured in a horizontal line (Col. 18, Line 53 to Col. 19, Lines 8). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in Clothier/Asai, the circuit carrier is manufactured in a

horizontal line, as taught by Yokogawa et al., in order to simplify the process of manufacture the printed circuit board.

30. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clothier et al. (US Pub. 2002/0177006) in view of Asai et al. (US Pat. 6,240,636) and further view of Frank et al. (US Pat. 5,577,309) (newly cited).

31. Regarding claim 23, Clothier/Asai disclose all the claimed features as set forth above including from Asai, the vias (5, Fig. 1) have a V shape cross section **except** the trenches have a V-shape cross section. Frank et al. discloses the trenches 22 (Fig. 1) and (23, Fig. 1) have a V-shape cross section. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in Clothier/Asai, the trenches have a V-shape cross section, in order to simply the laser etching step.

32. Applicant's arguments, filed 4/5/2020, with respect to claim 1and 12 have been fully considered and are persuasive. The rejection of claim 1 and 12 has been withdrawn.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUNG NGUYEN whose telephone number is (571)270-7828. The examiner can normally be reached on Monday-Friday, 9M-6PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tu Hoang can be reached on (571)272-4780. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUNG NGUYEN/
Examiner, Art Unit 3742
6/19/2010
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